2013-2014, VMDS, M.Tech (VLSI) I Sem

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
1	17/10/13	An overview of design procedure and fpga system designing CAD TOOLS	I	CL		
2	18/10/13	Design entry synthesis, simulation, optimization	I	"		
3	18/10/13	place and route, design verification tools.	I	"		
4	24/10/13	Examples using commercial PC based on VHDL/Hardware	I	"		
5	25/10/13	Top down design with VHDL Subprograms.	I	"		
6	25/10/13	Controller description VHDL operators.	I	"		
7	31/10/13	Characterizing Hardware languages.	II	"		
8	7/11/13	Objects and classes, signal Assignments.	II	"		
9	8/11/13	Concurrent and sequential Assignments.	II	"		
10	8/11/13	Structural Specification of hardware.	II	"		
11	14/11/13	parts Library wiring of primitives	II	"		
12	15/11/13	wiring interactive Networks	II	"		
13	15/11/13	modeling A Test Bench Binding	II	"		
14	21/11/13	A Test bench Binding Alternative Top down wiring	II	"		
15	22/11/13	design Organization and Parameterization	III	"		
16	22/11/13	definition and usage of subprograms.	III	"		
17	28/11/13	packaging parts and utilities	III	"		
18	29/11/13	design parameterization	III	"		
19	29/11/13	design configuration	III	"		
20	5/12/13	design Libraries	III	"		

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21	6/12/13	Utilities for High-level description - Type declaration	IV	CL		
22	6/12/13	Unask, VHDL operators	IV	"		
23	12/12/13	Sub program parameters Types	IV	"		
24	13/12/13	Subprogram overloading	IV	"		
25	13/12/13	other types and Type related issues	IV	"		
26	14/12/13	predefined Attributes, User defined Attributes	IV	"		
27	19/12/13	packing Basic Utility	IV	"		
28	20/12/13	multiplexing and data selecting state machine description	V	"		
29	20/12/13	open collector gates, Three state BUSSing Agency data flow	V	"		
30	26/12/13	updating basic utilities, Behavioral description of hardware	V	"		
31	27/12/13	process Statement as selection statements with sequential statements.	V	"		
32	27/12/13	formated ASSI I/O operations, MSI-based design	V	"		
33	2/1/14	Pakman CPU, Behavioral description of pakman	VI	"		
34	3/1/14	BUSSing Structure, Data flow description.	VI	"		
35	3/1/14	Test bench for the pakman CPU.	VI	"		
36	5/1/14	A more realistic pakman. Final	VI	"		
37	5/1/14	Interface design and modeling.	VI	"		
38	9/1/14	VHDL AS A modeling languages	VI	V		