LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective ... Upon Re...
		UNIT-I				
		Operational Amplifiers	I			
1	17.10.13	General considerations one stage op-Amps, two-		CR		
		stage op-Amp gain				
2	18.10.13	Boosting stage compensation i/p range limitation		CR		
		Slew rate				
		CURRENT MIRRORS, SINGLE STAGE AMPLIFIERS	I			
3	18.10.13	simple CMOS, BJT current Mirror		CR		
4	24.10.13	cascode wilson wilder current mirror		CR		
5	25.10.13	Common source follower common gate Amplifier		CR		
		NOISE	I			
6	25.10.13	Types of noise, thermal noise Flicker noise		CR		
		Noise in op-Amp				
7	30.10.13	Noise in common source stage & NMR		CR		
		Band width				
		UNIT-II	II			
		PHASE Locked Loop design				
8	31.10.13	PLL concepts PLL Loop in the Locked Range condition		CR		
		Integrated circuits, PLL's phase detector				
9	01.11.13	VCO case study, Analysis of 560B monolithic		CR		

PLL

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		UNIT - III				
		SWITCHED CAPACITOR CIRCUITS	III			
10	01.11.13	Basic Building Blocks op-amps capacitor switches		OR		
		Non-overlapping capacitors				
11	07.11.13	Basic operation and Analysis - register		OR		
		equivalance of switch capacitor				
12	08.11.13	parasitic sensitive Integrator and parasitic		OR		
		Insensitive Integrator signal Flowgraph Analysis				
13	08.11.13	First order Filter switch sharing, Fully differential		OR		
		filters charged Injection				
14	21.11.13	switched capacitor gain circuits, parallel		OR		
		resistor capacitor circuit				
15	22.11.13	precise table gain circuit, other switched capacitor		OR		
		circuits; Full wave rectifier peak detector sinusoidal oscillator				
		UNIT - IV	IV			
		LOGIC FAMILIES AND CHARACTERISTICS				
16	22.11.13	CMOS, TTL, ECL Logic families		PPT		
17	27.11.13	CMOS/TTL Interfacing comparision of Logic		PPT		
		families				

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		UNIT - IV COMBINATIONAL LOGIC DESIGN USING VHDL	IV			
18	28.11.13	VHDL modelling for Decoder, Encoder multiplexer		PPT		
19	29.11.13	Comparision Adder and subtractor		PPT		
		SEQUENTIAL DESIGN using VHDL	II			
20	29.11.13	VHDL modelling for latches, D/F/s counter,		PPT		
		Shift registers				
21	05.12.13	FSM, ASM chart		PPT		
		UNIT - V				
		DIGITAL INTEGRATED SYSTEMS BUILDING BLOCKS	V			
22	05.12.13	Multiplexer and Decoder		PPT		
23	06.12.13	Barrel shifter, counter Digital single bit Adder		PPT		
		MEMORIES	V			
24	11.12.13	Ram Internal structure 2D-decoding Comparator		PPT		
		type timing and Application				
25	12.12.13	RAM Internal structure		PPT		
		CPLD	V			
26	13.12.13	XC 9500 series family CPLD structure		PPT		
		CLB Internal structure				
27	13.12.13	I/O Block Internal structure		PPT		

iod	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		FPGA	V			
28	19.12.13	Conceptual overview of FPGA		PPT		
29	20.12.13	classification based on CLB Internal Architecture				
		I/O block Architecture		PPT		
		UNIT-VI				
		COMPARATORS				
30	20.12.13	Wing of-Amp as a comparator, Chargi	VI	CR		
		Injection error latch comparator				
		NYQUIST RATE DIA CONVERTERS	VI			
31	26.12.13	Decoder based counter Resistor String converter		CR		
32	27.12.13	Folded Register, String converter, Binary scaled		CR		
		converter				
33	29.12.13	Binary weighted Register converter, Reduced		CR		
		Rishna Ratio Ladder				
34	03.01.14	R-2R based conver- Thermo meter code		CR		
		circuit mock DIA converter				
		NYQUIST RATE A/D CONVERTER	VI			
35	04.01.14	Integrating converter, Successive approximation		CR		
		converter				
36	04.01.14	DAC based Sentive Approximation, Flash converter		CR		

Time Interleaved A/D converter