LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1		Important Concepts in VERILOG : Basics of Verilog Language	I	Black Board		
2		Operators	"	"		
3		Hierarchy	"	"		
4		Procedures and Assignments	"	"		
5		Timing Controls and Delay	"	"		
6		Tasks and Functions Control statements	"	"		
7		Logic Gate Modeling	"	"		
8		Modeling Delay	"	"		
9		Altering Parameters	"	"		
10		Other Verilog Features	"	"		
11		Synthesis And Simulation Using HDLs-Verilog & Logic Synthesis	II	Black Board		
12		VHDL And Logic Synthesis	"	"		
13		Memory Synthesis	"	"		
14		FSM Synthesis	"	"		
15		Memory Synthesis	"	"		
16		Performance-Driven Synthesis	"	"		
17		Simulation - Types of Simulation	"	"		
18		Logic Systems Working of Logic Simulation	"	"		
19		Synthesis & Simulation Using HDLs - 2: Cell Models	III	Black Board		
20		Delay Models State Timing Analysis	"	"		

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21		Formal Verification	"	"		
22		Switch-level Simulation Transistor-level Simulation	"	"		
23		CAD Tools for synthesis & Simulation Modelsim & Leonardo Spectrum	"	"		
24		Pspice Models for Transistors	IV	Black Board		
25		A/D & D/A sample and Hold circuits	"	"		
26		Digital System Building Blocks	"	"		
27		Design and Analysis of Analog & Digital circuits	"	"		
28		Fundamental of Analog & Digital Simulation	V	Black Board		
29		Mixed Signal Simulator Configurations	"	"		
30		Understanding Modeling	"	"		
31		Integration to CAE Environments	"	"		
32		Analyses of Analog circuits Eg. A/D, D/A converters	"	"		
33		UP and Docon Converters	"	"		
34		Compounders Etc	"	"		
35		An overview of High Speed PCB Design	VI	BB		
36		Design Entry	"	"		
37		Simulation and Layout Tools for PCB	"	"		
38		Introduction to Orcad PCB Design Tools	"	"		