LESSON PLAN

Subject Code & Name: Digital System Design

Branch: VLSI & DECS   Class / Semester: IM.Tech-SEM 1   Academic Year:2013-14
Faculty: J.Swathi

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective action upon review
		DESIGN OF DIGITAL SYSTEMS	**I**			
1	17/10/13	Introduction		BB		
2	18/10/13	ASM charts		BB		
3	18/10/13	Data path design Control logic implementation		BB		
4	23/10/13	Equivalent states and state tables		BB		
5	24/10/13	Reduction of state tables- Row matching method		BB		
6	25/10/13	Guidelines for state assignments		BB		
		SEQUENTIAL CIRCUIT DESIGN	**II**			
7	25/10/13	Design of iterative circuits		BB		
8	30/10/13	Introduction to ROM & PLA		BB		
9	31/10/13	Design of sequential circuits using ROM		BB		
10	01/11/13	Design of sequential circuits using PLA		BB		
11	01/11/13	Design of sequential circuits using FPGA		BB		
12	06/11/13	Design of sequential circuits using CPLD		BB		
		FAULT MODELING	**III**			
13	07/11/13	Fault classes and models		BB		
14	08/11/13	Stuck at faults, Bridging faults Transition and Intermittent faults		BB		
15	08/11/13	State identificationc experiments – successor tree		BB		
16	20/11/13	Machine identification experiments		BB		
17	20/11/13	Fault detection experiments		BB		
		TEST PATTERN GENERATION	**IV**			
18	21/11/13	Test generation-Fault table method		BB		
19	22/11/13	Path sensitization Algorithm		BB		
20	22/11/13	Boolean difference method		BB		
21	27/11/13	Kohavi Algorithm		BB		
22	28/11/13	D-Alogorithm		BB		
23	29/11/13	PODEM		BB		
24	29/11/13	Random testing		BB		

25	05/12/13	Transition count testing		BB			
26	06/12/13	Signature analysis		BB			
27	06/12/13	Testing for bridging faults		BB			
		PROGRAMMING LOGIC ARRAYS	**V**				
28	12/12/13	Introduction to PLA		BB			
29	13/12/13	Design using PLA		BB			
30	13/12/13	PLA Minimization		BB			
31	19/12/13	PLA Folding-Row & column folding		BB			
32	20/12/13	PLA Testing		BB			
33	20/12/13	Fault models in PLA		BB			
34	25/12/13	Test generation for PLA		BB			
35	26/12/13	Testable PLA design		BB			
		ASYNCHRONOUS SEQUENTIAL MACHINE	**VI**				
37	27/12/13	Fundamental mode model		BB			
38	27/12/13	Flow table, primitive flow table		BB			
39	02/01/14	State reduction		BB			
40	02/01/14	Minimal closed covers,Races		BB			
41	03/01/14	Cycles,hazards		BB			

CR: CLASS ROOM   **PPT: POWER POINT PRESENTATION**   **LCD**

TEXT BOOKS:
1. Z. Kohavi – "Switching & finite Automata Theory" (TMH).
2. N. N. Biswas – "Logic Design Theory" (PHI).
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCE BOOKS:
1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications.
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition.

FACULTY   **HEAD OF THE DEPARTMENT**